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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,931	02/26/2002	Arjun P. Chandran	P-7433	8349

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EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,931	CHANDRAN ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *21-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *2/10/05* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 23 are presented for examination.

Election/Restrictions

2. During a telephone conversation with Mr. Philip J. McKay on 10 February 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1 – 20. Affirmation of this election must be made by applicant in replying to this Office action. Claims 21 – 23 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1 - 20, drawn to energy saving, classified in class 713, subclass 600.

II Claims 21 - 23, drawn to network device, classified in class 712, subclass 218;226-227, and 234.

4. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as an apparatus and method of operation of a modified glitch latch. In the instant case,

invention II has separate utility such as a method for performing conditional read operation of a retirement payload array in a microprocessor. See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

7. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 1 – 20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 24 of U.S. Patent

Application Publication No. US 2003/0154365 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention of conditional read including a modified glitch latch/logic circuit that opens an output only when both clock signal and a read signal are in active phase.

10. Every elements of claim 1, in current application including a latch circuit with a clock and read inputs, output conditions including clock signal in "B" phase and read signal in active phase are taught by claims 5, and 8 of copending application.

11. The sensing element of claim 2, in current application is taught by claims 5, 11, and 8 of copending application.

12. Elements of claims 3 – 5, in current application are taught by claims 3, 6 – 7, and 5, of copending application.

13. Every elements of claim 6, in current application including a logic arrangements with logical circuit including inverter, NAND, OR, NOR gates are taught by claims 8, 16, and 21 of copending application.

14. Elements of claim 7, in current application including coupling of sensing element coupled with read word line of RPA [retirement Payload Array] with shift in position are taught by claims 11, and 12 - 13, of copending application.

15. Elements of claims 8 – 10, in current application are taught by claims 12 – 15, and 17 – 20, of copending application.

16. Every elements of claim 11, in current application including logic arrangements with logical circuit including inverter, and NAND, gates are taught by claim 16 of copending application.

17. The sensing element of claim 12, in current application is taught by claims 13, and 15 of copending application.

18. Elements of claims 13 – 15, in current application are taught by claims 12 – 15, and 17 – 20, of copending application.

19.

20. Elements of claim 17, in current application including coupling of sensing element coupled with read word line of RPA [retirement Payload Array] with shift in position are taught by claims 11, and 12 - 13, of copending application.

21. Elements of claims 18 – 20, in current application are taught by claims 3 – 5, and 7 of copending application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1 – 5, and 16 – 20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kanazashi et al. [hereinafter as Kanazashi], US Patent 6,337,833 B1.

2. As to claim 1, Kanazashi discloses a modified glitch latch [a circuit configuration for generating controlled clock signal, fig. 3] comprising:

a. a modified glitch latch output terminal [CLK1];

b. a control circuit [72, clock supply control signal generator], said control circuit comprising control circuit first input terminal [I-CLK], a control circuit second input terminal [READ] and control circuit output terminal [READCZ];

c. a clock signal [I-CLK] coupled to said control circuit first input terminal, said clock signal having a first or "A" phase [falling edge] and a second or " B " phase [rising edge];

d. a read signal [READ] coupled to said control circuit second input terminal, said read signal having a first inactive phase [LOW] and a second or active phase [HIGH], wherein;

e. a control signal [READCZ] from said control circuit output terminal [CLK1] opens said modified glitch latch only when both:

(i) said clock signal is in said "B" phase [rising edge] ; and

(ii) said read signal is in said active phase [HIGH][col. 4, lines 57 – 67,col. 5, lines 1 – 10, 55 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 38, fig. 3 – 6].

3. As to claim 16, Kanazashi discloses a method for controlling the operation of modified glitch latch [a circuit configuration for generating controlled clock signal, fig. 3] comprising:

a. receieving a clock signal [I-CLK], said clock signal having a first or "A" [falling edge] phase and a second or "B", phase [rising edge];

b. receiving a read signal [READ], said read signal having a first or inactive phase [LOW] and a second or active phase [HIGH]; and

c. opening said modified glitch latch only when, both:

(i) said clock signal is in said "B" phase [rising edge]; and

(ii) said read signal is in said active phase [HIGH][col. 4, lines 57 – 67,col. 5, lines 1 – 10, 55 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 38, fig. 3 – 6].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 2 – 5, and 17 – 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi et al. [hereinafter as Kanazashi], US Patent 6,337,833 B1 as applied to claims 1, and 16 above, and further in view of Wallace Steven et al. Design and Implementation of a 100 MHz Reorder Buffer, IEEE, 1995 [hereinafter as Wallace].

5. As to claims 5, and 17, Kanazashi discloses a modified glitch latch [a circuit configuration for generating controlled clock signal, fig. 3] comprising: a modified glitch latch output terminal [CLK1]; a control circuit [72, clock supply control signal generator], said control circuit comprising control circuit first input terminal [I-CLK], a control circuit second input terminal [READ] and control circuit output terminal [READCZ]; a clock signal [I-CLK] coupled to said control circuit first input terminal, said clock signal having a first or "A" phase [falling edge] and a second or " B " phase [rising edge]; a read signal [READ] coupled to said control circuit second input terminal, said read signal having a first inactive phase [LOW] and a second or active phase [HIGH], wherein; a control signal [READCZ] from said control circuit output terminal [CLK1] opens said modified glitch latch only when both: (i)said clock signal is in said "B" phase [rising edge] ; and (ii)said read signal is in said active phase [HIGH][col. 4, lines 57 – 67,col. 5, lines 1 – 10, 55 – 67, col. 6, lines 1 – 67, col. 7, lines 1 – 38, fig. 3 – 6].

However, Kanazashi teaches the use of circuit configuration [latch] for memory device but does not teach explicitly use with a read word line of a retirement payload array. In summary, he does not teach read word line of a retirement payload array.

Wallace teaches a retirement payload array with receiving an advance pointer signal, said advance pointer signal having a first or inactive phase and a second or active phase, said second or active phase of said advance pointer signal corresponding to a shift in position of a read pointer of said retirement payload array [Page 45, Figure 7, MATCH LOCAL, pages 42-44]; initiating a read of said retirement payload array only when, both: (i) clock signal is in said "B" phase [page 45, Figure 7], and (ii) advance

pointer signal is in said active phase [page 45, Figure 7]; and wherein, each of said pre-charge devices is a transistor [Page 44, precharge control transistor] and each of said sensing devices is a latch [Page 43, Figure 3, Shift cell is a flip-flop].

It would have been obvious to one of ordinary skill in art, having the teachings of Kanazashi and Wallace before him at the time of invention was made, to modify use of configuration circuit as disclosed by Kanazashi to include use of reorder buffer with a read word line of retirement pay load array as taught by Wallace, in order to obtain a superscalar microprocessor architecture that allows out-of-order issue and completion of instructions which contribute to overall performance enhancement [abstract].

6. As to claims 6, and 18, Wallace teaches retirement payload array comprises M read word lines and N read bit lines further wherein [page 44], each of said N read bit lines coupled to a corresponding pre-charge device [Page 45, Data cells are pre-charged] and a corresponding sensing device [Page 43, Figure 3, Shift Cell].

7. As to claims 4 – 5, and 19 – 20, Wallace teaches retirement pay load array with M read word lines and N read bit lines, as described above therefore he teaches different number of rows including M is equal to 16 and number of columns N is equal to 192 too.

8. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested to the applicant in preparing responses, to

fully consider the references in entirely as potentially teaching all or part of claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

9. **Prior Art not relied upon:** Please refer to the references listed in attached PTO-892 which, are not relied upon for rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am to 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Nitin C. Patel
February 14, 2005